# On Timed-Automata semantics for ARTS

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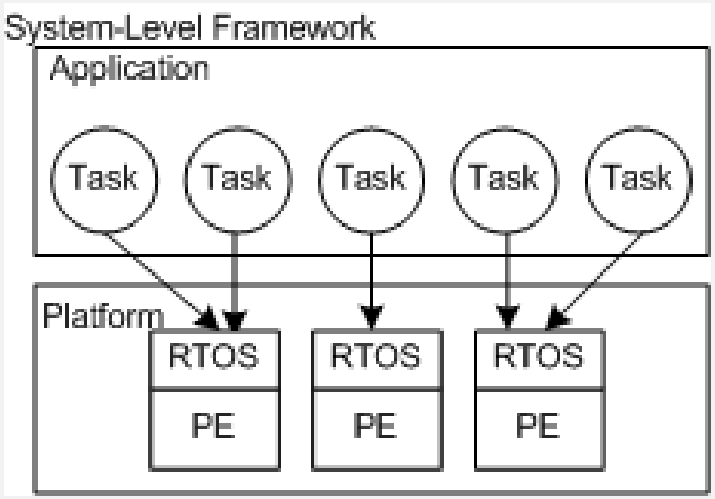
# The ARTS modelling framework

ARTS: A system-level MPSoC simulation framework

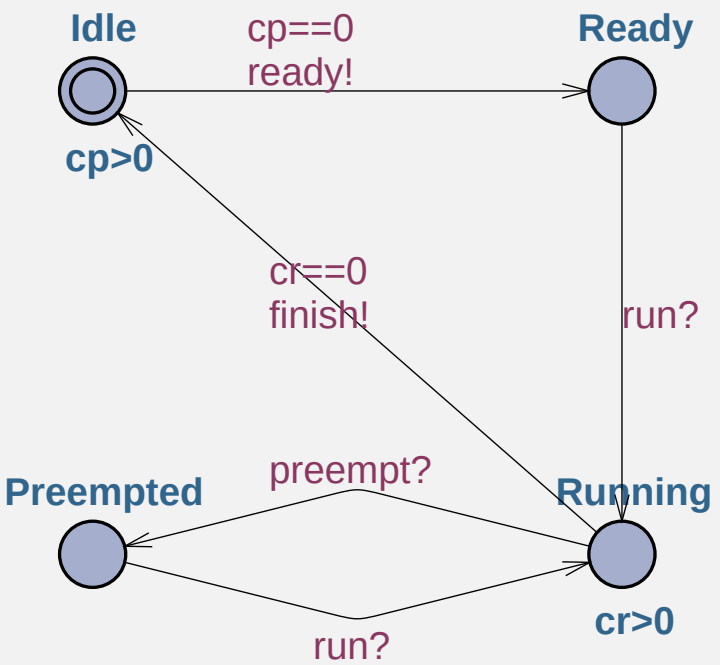



- Properties of the solution depends on the design of the application as well as the configuration of the platform.

design space exploration

# A simplified task in ARTS

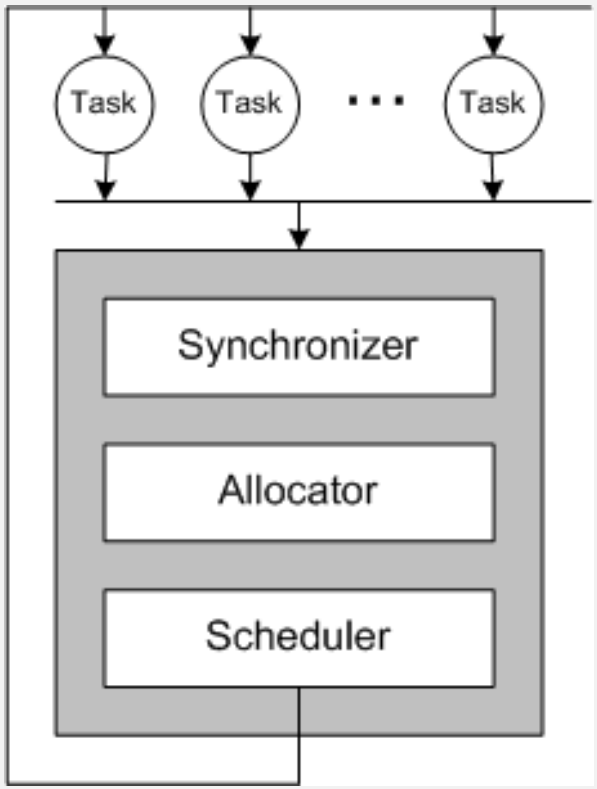
- Simple periodic tasks, which can be preempted




- cp, cr: time-dependent variables for the period and run time

semi-formal framework: much implicit information

# ARTS model of a processing element




- Synchronizer — resolves dependencies before task selection
- Allocator — grants access to shared resources (busses, memories, ...)
- Scheduler — grants processor time to tasks according to some scheduling discipline

- Components are informally described and implemented in SystemC
- ARTS is a simulation framework only

# Timed-Automata models for ARTS

First set of goals:

- Precise definition of components and their communication, which can be communicated and discussed.
- Simulation (using UPPAAL) on a formal basis.
- Verification on a formal basis.

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An ARTS system is modelled as follows:

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\mathit{System} &= \mathit{Application} \parallel \mathit{Platform} \\
\mathit{Application} &= \parallel_{i=1}^{n} \mathit{Task}_i \\
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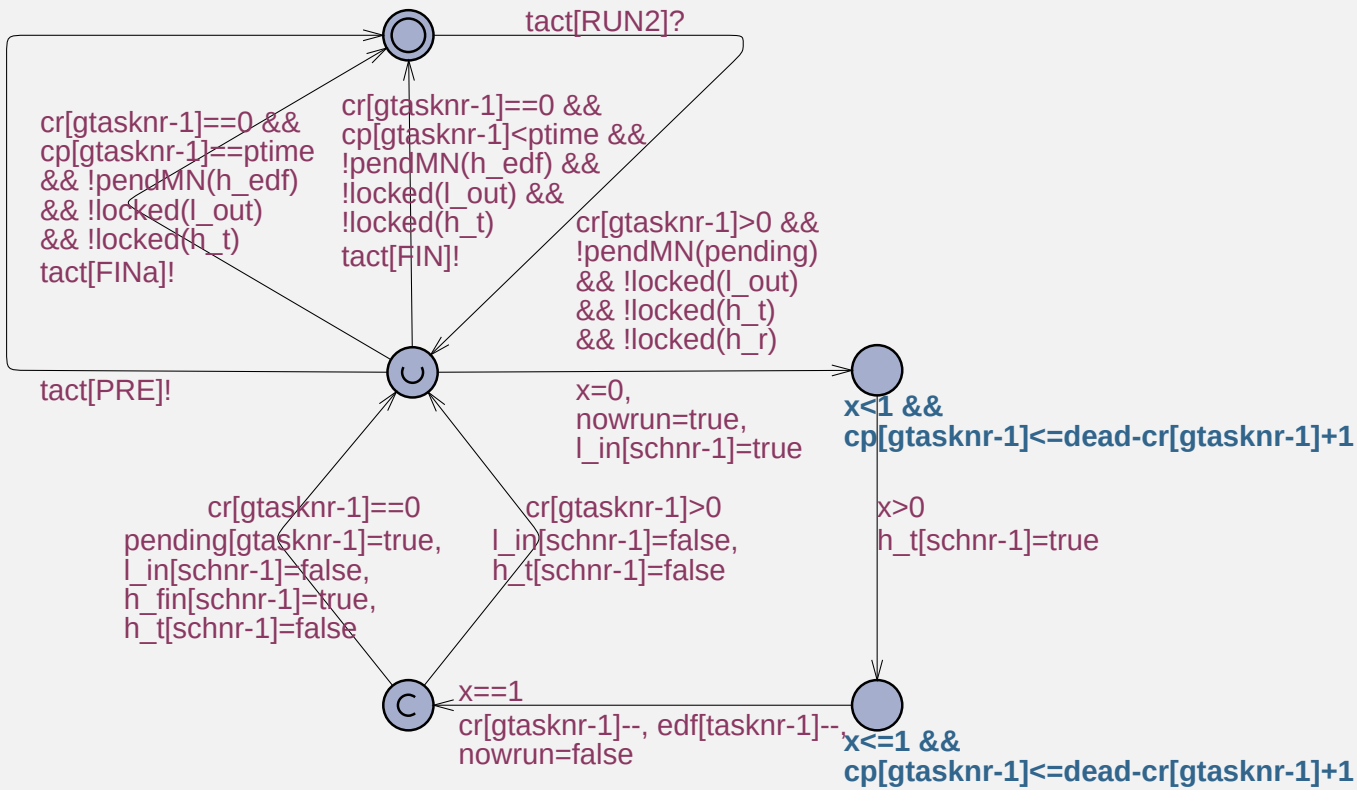
Each TA is approaching a comprehensible form

# Example TA: Running

- As an illustration of the level for complexity

The Running state of ARTS is expanded to:



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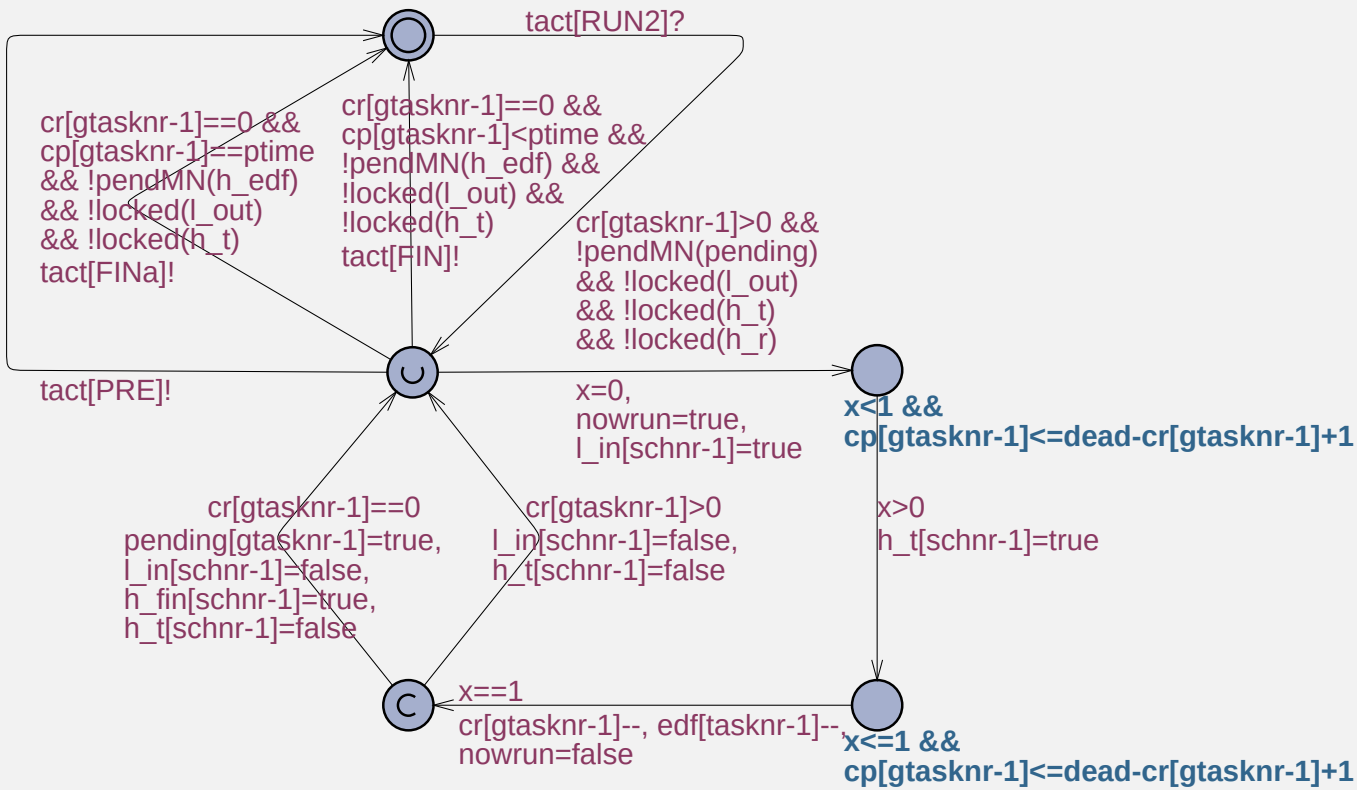


- discretization of running time to cope with preemption.

# Status

- Simple model with
  - multiple processing elements, cyclic tasks, causal dependencies among tasks.
  - Scheduling disciplines: earliest deadline first, rate-monotonic scheduling, fixed priority scheduling, deadline-monotonic scheduling.
- Verification of a collection of small problems.
  - Up to 11 tasks on up to 6 processors are verified within 1.5 min on a small PC.
  - Single processor case: examples are verified and compared to results from TIMES tool.
  - In the multiprocessor case: Small examples from the literature are verified.

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- "From specifications to task graphs"
- Case studies
- . . .